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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,669	OGAWA ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 02 December 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 20050211

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-4 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Referring to claims 1, and subsequently claims 2-4 and 9, Applicant has amended "defect information" to read "defective track information", rendering it unclear as whether this refers to "defect information" or "defective track information". As the invention has to do with pointing and referencing specific pieces of information, this amounts to a serious obstacle to the proper interpretation of the claims.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 5-8, 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by US 4498146 to Martinez. Referring to claim 5, Martinez discloses a storage means that has an area in which pieces of physical track number information on defective tracks are stored in to areas at respective addresses corresponding to said pieces of physical track number information, and an area in which pieces of defect information on said defective tracks are stored (From line 21 of column 8, "If the virtual address is valid, the DFC processor 14 undertakes the translation thereof into a real address. As shown by block 38, the DFC processor 14 stores the virtual address in a variable referred to as an

incremented virtual address (IVA) 20. The IVA 20 is a memory location in the DFC RAM 15b (see FIG. 4) which is utilized for temporary storage by the DFC controller 14. Alternatively, the IVA 20 may be a general register (not shown) within the DFC controller 14. As further shown by the block 38, the DFC controller 14 also initializes the contents P of a defect table pointer 32 in the active job table (AJT) 25a. The defect table pointer 32 points to an entry in the defect table 24a which contains the address of the next defect that must be considered in the current translation process."); and a processing means for receiving an instruction of read or write to a track of said storage medium, for referring to said storage means, and for performing defect processing on a defective track (From line 27 of column 3, "The DFC 12 may be any suitable commercially available unit. The DFC 12 operates in a conventional manner, with exceptions that are explained further below. Inter alia, the DFC 12 includes a DFC processor 14 and a DFC memory 15. The DFC processor 14 initiates and responds to signaling that makes up the communication protocol of the bus 18 and actively controls the operation of the disk file 13, including the accessing of storage locations therein for purposes of writing information into or reading information out of those locations. The DFC memory 15 is a rapidly accessible memory. The time for access by the DFC processor 14 of a memory location in the DFC memory 15 is significantly lower than its time for access of a memory location in the disk file 13. The DFC memory 15 is comprised of two portions: a readable and writable, random access, memory (RAM) 15b and a readable-only memory (ROM) 15a. The DFC ROM 15a holds the program under whose control the DFC processor 14 operates. The program includes the various

routines, flowcharted in FIGS. 5-10, that the DFC processor 14 executes. The DFC RAM 15 b holds the data required by the DFC processor 14 for operation, and also provides buffer storage for information being transferred between the disk file 13 and the system bus 18."); and said storage means stores said pieces of physical track number information on defective tracks and pieces of pointer information indicating addresses of areas at which pieces of defect information on said defective tracks are stored (From line 21 of column 8, "If the virtual address is valid, the DFC processor 14 undertakes the translation thereof into a real address. As shown by block 38, the DFC processor 14 stores the virtual address in a variable referred to as an incremented virtual address (IVA) 20. The IVA 20 is a memory location in the DFC RAM 15b (see FIG. 4) which is utilized for temporary storage by the DFC controller 14. Alternatively, the IVA 20 may be a general register (not shown) within the DFC controller 14. As further shown by the block 38, the DFC controller 14 also initializes the contents P of a defect table pointer 32 in the active job table (AJT) 25a. The defect table pointer 32 points to an entry in the defect table 24a which contains the address of the next defect that must be considered in the current translation process."); and when said processing means receives an instruction of read or write to a track of said storage medium, said processing means refers to a piece of said physical track number information on defective tracks based on said addresses, and then, when said track as an object of said instruction is a defective track, refers to a piece of said pointer information, to detect a piece of the defect information at a storage area indicated by said piece of the pointer information, **said piece of defect information having a plurality of formats**

for processing a plurality of defects (From the abstract (with emphasis), "During use of the disk, the disk file controller reads the table of defects into its memory and uses it to translate virtual addresses into real addresses. The translation process skips over real addresses of defective locations. The virtual address is translated into a real address by being **incremented by the number of defects** whose addresses are lower than the real address. Subsequent contiguous virtual addresses are translated into real addresses by being incremented by the number of **contiguous defective locations** that follow the location associated with the preceding virtual address." Further, from line 31 of column 7, "As it is not desirable to access defective storage locations, the real addresses of the defective locations cannot be assigned to any virtual addresses. For example, **contiguous virtual addresses** may have to be converted into **noncontiguous real addresses** to avoid associating the real address of a defective physical storage location with the virtual address of a valid and usable logical storage location."), and performs defect processing on said defective track based on said piece of the defect information (From line 6 of column 8, "To convert the virtual address into a real address, the DFC processor 14 performs the operations flowcharted in FIG. 7. Having received the virtual address (VA), as shown in block 36, the DFC processor 14 first checks whether the address is a valid virtual address, as shown in block 37. Validity of the address is determined by whether or not the given virtual address is exceeded by the virtual address of the last storage location in the disk 13a which is available for use by a job. The address of the last available storage location in the disk media 50 is determined by the DFC processor 14 from the disk type 33 entry of the AJT

25a. If the virtual address is invalid, the DFC processor 14 aborts the job, as shown in block 66, and sends a message to the originator of the job informing it thereof. If the virtual address is valid, the DFC processor 14 undertakes the translation thereof into a real address. As shown by block 38, the DFC processor 14 stores the virtual address in a variable referred to as an incremented virtual address (IVA) 20. The IVA 20 is a memory location in the DFC RAM 15b (see FIG. 4) which is utilized for temporary storage by the DFC controller 14. Alternatively, the IVA 20 may be a general register (not shown) within the DFC controller 14. As further shown by the block 38, the DFC controller 14 also initializes the contents P of a defect table pointer 32 in the active job table (AJT) 25a. The defect table pointer 32 points to an entry in the defect table 24a which contains the address of the next defect that must be considered in the current translation process. As no defects have yet been considered, the defect table pointer 32 is initialized to point to the first entry 27 of the defect table 24a, by being loaded with the contents of the DTA 31. Likewise as shown in the block 38, the processor 14 also resets to zero the contents d of a defect counter 26." Further, from line 15 of column 9, "As shown by the block 41, the DFC processor 14 increments the contents P of the defect table pointer 32 by the count d of the counter 26 to point the pointer 32 to the first entry of the defect table 24a which exceeds the virtual address. The DFC processor 14 also increments the IVA 20 by the count d of the counter 26 to shift the virtual address and thus compensate it for the number of defective storage locations whose real addresses precede the virtual address.").

5. Referring to claim 6, Martinez discloses said storage means partitions a storage area into partition areas each corresponding to a plurality of tracks, and further stores pieces of identification information on said partition areas; and said processing means accesses each of said partition areas each corresponding to a plurality of tracks (From line 52 of column 3, "The disk file 13 is comprised of one or more disks. In the example of FIG. 1, the disk file 13 includes up to eight disks 13a-13h. The disks 13a through 13h may be conventional commercially available units. Each disk 13a through 13h operates independently of the others. The disks 13a through 13h are substantially the same, and therefore only one, the disk 13a, will be discussed in more detail, with the understanding that the discussion pertains to the disks 13b through 13h as well.").

6. Referring to claim 7, Martinez discloses a storage means for storing pieces of physical track number information on defective tracks and pieces of defect information on said defective tracks into areas at respective addresses corresponding to said pieces of physical track number information (From line 21 of column 8, "If the virtual address is valid, the DFC processor 14 undertakes the translation thereof into a real address. As shown by block 38, the DFC processor 14 stores the virtual address in a variable referred to as an incremented virtual address (IVA) 20. The IVA 20 is a memory location in the DFC RAM 15b (see FIG. 4) which is utilized for temporary storage by the DFC controller 14. Alternatively, the IVA 20 may be a general register (not shown) within the DFC controller 14. As further shown by the block 38, the DFC controller 14 also initializes the contents P of a defect table pointer 32 in the active job table (AJT) 25a. The defect table pointer 32 points to an entry in the defect table 24a which

contains the address of the next defect that must be considered in the current translation process."); and a processing means for receiving an instruction of read or write to a track of said storage medium, for referring to said storage means, and for performing defect processing on a defective track (From line 27 of column 3, "The DFC 12 may be any suitable commercially available unit. The DFC 12 operates in a conventional manner, with exceptions that are explained further below. Inter alia, the DFC 12 includes a DFC processor 14 and a DFC memory 15. The DFC processor 14 initiates and responds to signaling that makes up the communication protocol of the bus 18 and actively controls the operation of the disk file 13, including the accessing of storage locations therein for purposes of writing information into or reading information out of those locations. The DFC memory 15 is a rapidly accessible memory. The time for access by the DFC processor 14 of a memory location in the DFC memory 15 is significantly lower than its time for access of a memory location in the disk file 13. The DFC memory 15 is comprised of two portions: a readable and writable, random access, memory (RAM) 15b and a readable-only memory (ROM) 15a. The DFC ROM 15a holds the program under whose control the DFC processor 14 operates. The program includes the various routines, flowcharted in FIGS. 5-10, that the DFC processor 14 executes. The DFC RAM 15 b holds the data required by the DFC processor 14 for operation, and also provides buffer storage for information being transferred between the disk file 13 and the system bus 18."); and when said processing means receives an instruction of read or write to a track of said storage means, said processing means refers to a piece of said physical track number information on defective tracks based on

said addresses to detect a piece of the defect information, and then, when said track as an object of said instruction is a defective track, performs defect processing on said defective track based on said piece of the defect information, **said pieces of defect information having a plurality of formats for processing a plurality of defects** (From the abstract (with emphasis), "During use of the disk, the disk file controller reads the table of defects into its memory and uses it to translate virtual address**es** into real address**es**. The translation process skips over real addresses of defective locations. The virtual address is translated into a real address by being **incremented by the number of defects** whose addresses are lower than the real address. Subsequent contiguous virtual addresses are translated into real addresses by being incremented by the number of **contiguous defective locations** that follow the location associated with the preceding virtual address." Further, from line 31 of column 7, "As it is not desirable to access defective storage location**s**, the real address**es** of the defective location**s** cannot be assigned to any virtual address**es**. For example, **contiguous virtual addresses** may have to be converted into **noncontiguous real addresses** to avoid associating the real address of a defective physical storage location with the virtual address of a valid and usable logical storage location.") (From line 6 of column 8, "To convert the virtual address into a real address, the DFC processor 14 performs the operations flowcharted in FIG. 7. Having received the virtual address (VA), as shown in block 36, the DFC processor 14 first checks whether the address is a valid virtual address, as shown in block 37. Validity of the address is determined by whether or not the given virtual address is exceeded by the virtual address of the last storage location

in the disk 13a which is available for use by a job. The address of the last available storage location in the disk media 50 is determined by the DFC processor 14 from the disk type 33 entry of the AJT 25a. If the virtual address is invalid, the DFC processor 14 aborts the job, as shown in block 66, and sends a message to the originator of the job informing it thereof. If the virtual address is valid, the DFC processor 14 undertakes the translation thereof into a real address. As shown by block 38, the DFC processor 14 stores the virtual address in a variable referred to as an incremented virtual address (IVA) 20. The IVA 20 is a memory location in the DFC RAM 15b (see FIG. 4) which is utilized for temporary storage by the DFC controller 14. Alternatively, the IVA 20 may be a general register (not shown) within the DFC controller 14. As further shown by the block 38, the DFC controller 14 also initializes the contents P of a defect table pointer 32 in the active job table (AJT) 25a. The defect table pointer 32 points to an entry in the defect table 24a which contains the address of the next defect that must be considered in the current translation process. As no defects have yet been considered, the defect table pointer 32 is initialized to point to the first entry 27 of the defect table 24a, by being loaded with the contents of the DTA 31. Likewise as shown in the block 38, the processor 14 also resets to zero the contents d of a defect counter 26." Further, from line 15 of column 9, "As shown by the block 41, the DFC processor 14 increments the contents P of the defect table pointer 32 by the count d of the counter 26 to point the pointer 32 to the first entry of the defect table 24a which exceeds the virtual address. The DFC processor 14 also increments the IVA 20 by the count d of the counter 26 to

shift the virtual address and thus compensate it for the number of defective storage locations whose real addresses precede the virtual address.").

7. Referring to claim 8, Martinez discloses said storage means stores a volume of each piece of said defect information sequentially; and said processing means sequentially accesses said pieces of defect information (From line 7 of column 7, "Referring to FIG. 4, the defect table 24a comprises the ordered list of the addresses of defective tracks 54 existent in the disk media 50. The defect table 24a begins with an entry 27 designating the address of the first defective track 54 in the disk media 50 and continues with addresses of subsequent defects, down to an entry 28 which designates the address of the last defective track 54. The table 24a ends with an entry 29 which is the phantom address designating the end of the table 24a." Further, from the abstract, "A disk file controller uses manufacturer-provided information about the location of defects to construct a sequentially ordered list of addresses of defective storage locations in the disk, and the list is stored in a table in the disk. During use of the disk, the disk file controller reads the table of defects into its memory and uses it to translate virtual addresses into real addresses. The translation process skips over real addresses of defective locations. The virtual address is translated into a real address by being incremented by the number of defects whose addresses are lower than the real address. Subsequent contiguous virtual addresses are translated into real addresses by being incremented by the number of contiguous defective locations that follow the location associated with the preceding virtual address.").

8. Referring to claims 10 and 11, Martinez discloses said defect processing performs at least either of skipping processing, in which a defective sector is replaced by a normal sector, and slipping processing, in which a defective sector is replaced by a normal sector that physically follows said defective sector (From the abstract, "A disk file controller uses manufacturer-provided information about the location of defects to construct a sequentially ordered list of addresses of defective storage locations in the disk, and the list is stored in a table in the disk. During use of the disk, the disk file controller reads the table of defects into its memory and uses it to translate virtual addresses into real addresses. The translation process skips over real addresses of defective locations. The virtual address is translated into a real address by being incremented by the number of defects whose addresses are lower than the real address. Subsequent contiguous virtual addresses are translated into real addresses by being incremented by the number of contiguous defective locations that follow the location associated with the preceding virtual address.").

9. Referring to claims 12 and 13, Martinez discloses said pieces of defect information consist of control information and control contents, and said processing means grasps the format of the data for defect processing based on the control information and performs control processing in accordance with the format, whereby the defect processing on the defective tracks is performed based on the defect information (From the abstract, "A disk file controller uses manufacturer-provided information about the location of defects to construct a sequentially ordered list of addresses of defective storage locations in the disk, and the list is stored in a table in the disk. During use of

the disk, the disk file controller reads the table of defects into its memory and uses it to translate virtual addresses into real addresses. The translation process skips over real addresses of defective locations. The virtual address is translated into a real address by being incremented by the number of defects whose addresses are lower than the real address. Subsequent contiguous virtual addresses are translated into real addresses by being incremented by the number of contiguous defective locations that follow the location associated with the preceding virtual address.").

10. Referring to claims 14 and 15, Martinez discloses said format contains a sequential number of sectors as an object of the defect processing a plural number of times (From line 15 of column 9, "As shown by the block 41, the DFC processor 14 increments the contents P of the defect table pointer 32 by the count d of the counter 26 to point the pointer 32 to the first entry of the defect table 24a which exceeds the virtual address. The DFC processor 14 also increments the IVA 20 by the count d of the counter 26 to shift the virtual address and thus compensate it for the number of defective storage locations whose real addresses precede the virtual address." Further, from line 31 of column 7, "As it is not desirable to access defective storage locations, the real addresses of the defective locations cannot be assigned to any virtual addresses. For example, contiguous virtual addresses may have to be converted into noncontiguous real addresses to avoid associating the real address of a defective physical storage location with the virtual address of a valid and usable logical storage location.").

Response to Arguments

11. Applicant's arguments filed 2 December 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument regarding the processing of multiple defects using plural "formats", Martinez is shown to process contiguous physical sectors in the determination of a virtual address, such processing entailing the use of multiple data from the defect table for a single virtual address.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (571) 272-3645. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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